Mosfet Modeling For Vlsi Simulation Theory And Practice

MOSFET Models for VLSI Circuit SimulationMosfet Modeling For Vlsi Simulation: Theory And PracticeSemiconductor Device Modeling for VLSISemiconductor Device Modeling for VLSIHierarchical Modeling for VLSI Circuit TestingA One-Semester Course in Modeling of VSLI InterconnectionsTechnology Computer Aided DesignDigital VLSI Design and Simulation with VerilogCompact MOSFET Models for VLSI DesignConfiguration Management and Version Data Modeling in VLSI Design EnvironmentsAdvanced Model Order Reduction Techniques in VLSI DesignStatistical Performance Analysis and Modeling Techniques for Nanometer VLSI DesignsMulti-Level Simulation for VLSI DesignSemiconductor ProcessingCompact Models and Measurement Techniques for High-Speed InterconnectsModeling and Simulation of High Speed VLSI InterconnectsYield Simulation for Integrated CircuitsVLSI Fault Modeling and Testing TechniquesHardware Design and Simulation in VAL/VHDLStatistical Modeling for Computer-Aided Design of MOS VLSI Circuits Narain D. Arora Narain Arora Rachel Lee Kwyro Lee Debashis Bhattacharya Ashok Goel Chandan Kumar Sarkar Suman Lata Tripathi A. B. Bhattacharyya Sangchul Kim Sheldon Tan Ruijing Shen D.D. Hill Dinesh C. Gupta Rohit Sharma Michel S. Nakhla D.M. Walker George W. Zobrist Larry M. Augustin Christopher Michael
MOSFET Models for VLSI Circuit Simulation Mosfet Modeling For Vlsi Simulation: Theory And Practice Semiconductor Device Modeling for VLSI Semiconductor Device Modeling for VLSI Hierarchical Modeling for VLSI Circuit Testing A One-Semester Course in Modeling of VSLI Interconnections Technology Computer Aided Design Digital VLSI Design and Simulation with Verilog Compact MOSFET Models for VLSI Design Configuration Management and Version Data Modeling in VLSI Design Environments Advanced Model Order Reduction Techniques in VLSI Design Statistical Performance Analysis and Modeling Techniques for Nanometer VLSI Designs Multi-Level Simulation for VLSI Design Semiconductor Processing Compact Models and Measurement Techniques for High-Speed Interconnects Modeling and Simulation of High Speed VLSI Interconnects Yield Simulation for Integrated Circuits VLSI Fault Modeling and Testing Techniques Hardware Design and Simulation in VAL/VHDL Statistical Modeling for Computer-Aided Design of MOS VLSI Circuits *Narain D. Arora Narain Arora Rachel Lee Kwyro Lee Debashis Bhattacharya Ashok Goel Chandan Kumar Sarkar Suman Lata Tripathi A. B. Bhattacharyya Sangchul Kim Sheldon Tan Ruijing Shen D.D. Hill Dinesh C. Gupta Rohit Sharma Michel S. Nakhla D.M. Walker George W. Zobrist Larry M. Augustin Christopher Michael*

metal oxide semiconductor mos transistors are the basic building block ofmos integrated circuits i c very large scale integrated vlsi circuits using mos technology have emerged as the dominant technology in the semiconductor industry over the past decade the complexity of mos ic s has increased at an astonishing rate this is realized mainly through the reduction of mos transistor dimensions in addition to the improvements in processing today vlsi circuits with over 3 million transistors on a chip with effective or electrical channel lengths of 0 5 microns are in volume

production designing such complex chips is virtually impossible without simulation tools which help to predict circuit behavior before actual circuits are fabricated however the utility of simulators as a tool for the design and analysis of circuits depends on the adequacy of the device models used in the simulator this problem is further aggravated by the technology trend towards smaller and smaller device dimensions which increases the complexity of the models there is extensive literature available on modeling these short channel devices however there is a lot of confusion too often it is not clear what model to use and which model parameter values are important and how to determine them after working over 15 years in the field of semiconductor device modeling i have felt the need for a book which can fill the gap between the theory and the practice of mos transistor modeling this book is an attempt in that direction

a reprint of the classic text this book popularized compact modeling of electronic and semiconductor devices and components for college and graduate school classrooms and manufacturing engineering over a decade ago the first comprehensive book on mos transistor compact modeling it was the most cited among similar books in the area and remains the most frequently cited today the coverage is device physics based and continues to be relevant to the latest advances in mos transistor modeling this is also the only book that discusses in detail how to measure device model parameters required for circuit simulations the book deals with the mos field effect transistor mosfet models that are derived from basic semiconductor theory various models are developed ranging from simple to more sophisticated models that take into account new physical effects observed in submicron transistors used in today s 1993 mos vlsi technology the assumptions used to arrive at the models are emphasized so that the accuracy of the models in describing the device characteristics are clearly understood due to the importance of designing reliable circuits device reliability models are also covered understanding these models is essential when designing circuits for state of the art mos ics

explains basic semiconductor physics and looks at bipolar junction metal oxide semiconductor field effect and compound semiconductor field effect transistors thin film transistors and circuit simulation

test generation is one of the most difficult tasks facing the designer of complex vlsi based digital systems much of this difficulty is attributable to the almost universal use in testing of low gate level circuit and fault models that predate integrated circuit technology it is long been recognized that the testing prob lem can be alleviated by the use of higher level methods in which multigate modules or cells are the primitive components in test generation however the development of such methods has proceeded very slowly to be acceptable high level approaches should be applicable to most types of digital circuits and should provide fault coverage comparable to that of traditional low level methods the fault coverage problem has perhaps been the most intractable due to continued reliance in the testing industry on the single stuck line ssl fault model which is tightly bound to the gate level of abstraction this monograph presents a novel approach to solving the foregoing problem it is based on the systematic use of multibit vectors rather than single bits to represent logic signals including fault signals a circuit is viewed as a collection of high level components such as adders multiplexers and registers interconnected by n bit buses to match this high level circuit model we introduce a high level bus fault that in effect replaces a large number of ssl faults and allows them to be tested in parallel however by reducing the bus size from n

to one we can obtain the traditional gate level circuit and models

the optimum design of state of the art integrated circuits relies heavily on quantitative understanding of the parasitic capacitances and inductances in the resultant propagation delays and crosstalk phenomena associated with the metallic interconnections on the very large scale integrate circuits vsli this is because more than 65 of the delays on the integrated circuit chip occur in the interconnections and not in the transistors on the chip modeling of vsli interconnections will discuss the mathematical techniques necessary to model the parasitic capacitances inductances propagation delays crosstalk noise and electro migration induced failure associated with the interconnections in the realistic high density environment on a chip this book will be the first of its kind written for a one semester course on the mathematical modeling of metallic interconnections on a vlsi circuit in most institutions around the world this course will be offered at an upper level undergraduate and beginning graduate level the book will also be of interest to practicing engineers in the field who are looking for a quick refresher on the subject

responding to recent developments and a growing vlsi circuit manufacturing market technology computer aided design simulation for vlsi mosfet examines advanced mosfet processes and devices through tcad numerical simulations the book provides a balanced summary of tcad and mosfet basic concepts equations physics and new technologies related to tcad and mosfet a firm grasp of these concepts allows for the design of better models thus streamlining the design process saving time and money this book places emphasis on the importance of modeling and simulations of vlsi mos transistors and tcad software providing background concepts involved in the tcad simulation of mosfet devices it presents concepts in a simplified manner frequently using comparisons to everyday life experiences the book then explains concepts in depth with required mathematics and program code this book also details the classical semiconductor physics for understanding the principle of operations for vlsi mos transistors illustrates recent developments in the area of mosfet and other electronic devices and analyzes the evolution of the role of modeling and simulation of mosfet it also provides exposure to the two most commercially popular tcad simulation tools silvaco and sentaurus emphasizes the need for tcad simulation to be included within vlsi design flow for nano scale integrated circuits introduces the advantages of tcad simulations for device and process technology characterization presents the fundamental physics and mathematics incorporated in the tcad tools includes popular commercial tcad simulation tools silvaco and sentaurus provides characterization of performances of vlsi mosfets through tcad tools offers familiarization to compact modeling for vlsi circuit simulation r d cost and time for electronic product development is drastically reduced by taking advantage of tcad tools making it indispensable for modern vlsi device technologies they provide a means to characterize the mos transistors and improve the vlsi circuit simulation procedure the comprehensive information and systematic approach to design characterization fabrication and computation of vlsi mos transistor through tcad tools presented in this book provides a thorough foundation for the development of models that simplify the design verification process and make it cost effective

master digital design with vlsi and verilog using this up to date and comprehensive resource from leaders in the field digital vlsi design problems and solution with verilog delivers an expertly crafted treatment of the fundamental concepts of digital design and digital design verification with

verilog hdl the book includes the foundational knowledge that is crucial for beginners to grasp along with more advanced coverage suitable for research students working in the area of vlsi design including digital design information from the switch level to fpga based implementation using hardware description language hdl the distinguished authors have created a one stop resource for anyone in the field of vlsi design through eleven insightful chapters youll learn the concepts behind digital circuit design including combinational and sequential circuit design fundamentals based on boolean algebra youll also discover comprehensive treatments of topics like logic functionality of complex digital circuits with verilog using software simulators like isim of xilinx the distinguished authors have included additional topics as well like a discussion of programming techniques in verilog including gate level modeling model instantiation dataflow modeling and behavioral modeling a treatment of programmable and reconfigurable devices including logic synthesis introduction of plds and the basics of fpga architecture an introduction to system verilog including its distinct features and a comparison of verilog with system verilog a project based on verilog hdls with real time examples implemented using verilog code on an fpga board perfect for undergraduate and graduate students in electronics engineering and computer science engineering digital vlsi design problems and solution with verilogalso has a place on the bookshelves of academic researchers and private industry professionals in these fields

practicing designers students and educators in the semiconductor field face an ever expanding portfolio of mosfet models in compact mosfet models for vlsi design a b bhattacharyya presents a unified perspective on the topic allowing the practitioner to view and interpret device phenomena concurrently using different modeling strategies readers will learn to link device physics with model parameters helping to close the gap between device understanding and its use for optimal circuit performance bhattacharyya also lays bare the core physical concepts that will drive the future of vlsi development allowing readers to stay ahead of the curve despite the relentless evolution of new models adopts a unified approach to guide students through the confusing array of mosfet models links mos physics to device models to prepare practitioners for real world design activities helps fabless designers bridge the gap with off site foundries features rich coverage of quantum mechanical related phenomena si ge strained silicon substrate non classical structures such as double gate mosfets presents topics that will prepare readers for long term developments in the field includes solutions in every chapter can be tailored for use among students and professionals of many levels comes with matlab code downloads for independent practice and advanced study this book is essential for students specializing in vlsi design and indispensible for design professionals in the microelectronics and vlsi industries written to serve a number of experience levels it can be used either as a course textbook or practitioner s reference access the matlab code solution manual and lecture materials at the companion website wiley com go bhattacharyya

model order reduction mor techniques reduce the complexity of vlsi designs paving the way to higher operating speeds and smaller feature sizes this book presents a systematic introduction to and treatment of the key mor methods employed in general linear circuits using real world examples to illustrate the advantages and disadvantages of each algorithm following a review of traditional projection based techniques coverage progresses to more advanced mor methods for vlsi design including hmor passive truncated balanced realization tbr methods efficient inductance

modeling via the vpec model and structure preserving mor techniques where possible numerical methods are approached from the cad engineer s perspective avoiding complex mathematics and allowing the reader to take on real design problems and develop more effective tools with practical examples and over 100 illustrations this book is suitable for researchers and graduate students of electrical and computer engineering as well as practitioners working in the vlsi design industry

since process variation and chip performance uncertainties have become more pronounced as technologies scale down into the nanometer regime accurate and efficient modeling or characterization of variations from the device to the architecture level have become imperative for the successful design of vlsi chips this book provides readers with tools for variation aware design methodologies and computer aided design cad of vlsi systems in the presence of process variations at the nanometer scale it presents the latest developments for modeling and analysis with a focus on statistical interconnect modeling statistical parasitic extractions statistical full chip leakage and dynamic power analysis considering spatial correlations statistical analysis and modeling for large global interconnects and analog mixed signal circuits provides readers with timely systematic and comprehensive treatments of statistical modeling and analysis of vlsi systems with a focus on interconnects on chip power grids and clock networks and analog mixed signal circuits helps chip designers understand the potential and limitations of their design tools improving their design productivity presents analysis of each algorithm with practical applications in the context of real circuit design includes numerical examples for the quantitative analysis and evaluation of algorithms presented provides readers with timely systematic and comprehensive treatments of statistical modeling and analysis of vlsi systems with a focus on interconnects on chip power grids and clock networks and analog mixed signal circuits helps chip designers understand the potential and limitations of their design tools improving their design productivity presents analysis of each algorithm with practical applications in the context of real circuit design includes numerical examples for the quantitative analysis and evaluation of algorithms presented

and background 1 1 cad specification and simulation computer aided design cad is today a widely used expression referring to the study of ways in which computers can be used to expedite the design process this can include the design of physical systems architectural environments manufacturing processes and many other areas this book concentrates on one area of cad the design of computer systems within this area it focusses on just two aspects of computer design the specification and the simulation of digital systems vlsi design requires support in many other cad areas induding automatic layout ic fabrication analysis test generation and others the problem of specification is unique however in that it i often the first one encountered in large chip designs and one that is unlikely ever to be completely automated this is true because until a design s objectives are specified in a machine readable form there is no way for other cad tools to verify that the target system meets them and unless the specifications can be simulated it is unlikely that designers will have confidence in them since specifications are potentially erroneous themselves in this context the term target system refers to the hardware and or software that will ultimately be fabricated on the other hand since the functionality of a vlsi chip is ultimately determined by its layout geometry one might question the need for cad tools that work with areas other than layout

compact models and measurement techniques for high speed interconnects provides detailed analysis of issues related to high speed interconnects from the perspective of modeling approaches and measurement techniques particular focus is laid on the unified approach variational method combined with the transverse transmission line technique to develop efficient compact models for planar interconnects this book will give a qualitative summary of the various reported modeling techniques and approaches and will help researchers and graduate students with deeper insights into interconnect models in particular and interconnect in general time domain and frequency domain measurement techniques and simulation methodology are also explained in this book

modeling and simulation of high speed vlsi interconnects brings together in one place important contributions and state of the art research results in this rapidly advancing area modeling and simulation of high speed vlsi interconnects serves as an excellent reference providing insight into some of the most important issues in the field

in the summer of 1981 i was asked to consider the possibility of manufacturing a 600 000 transistor microprocessor in 1985 it was clear that the technology would only be capable of manufacturing 100 000 200 000 transistor chips with acceptable yields the control store rom occupied approximately half of the chip area so i considered adding spare rows and columns to increase rom yield laser programmed polysilicon fuses would be used to switch between good and bad circuits since only half the chip area would have redundancy i was concerned that the increase in yield would not outweigh the increased costs of testing and redundancy programming the fabrication technology did not yet exist so i was unable to experimentally verify the benefits of redundancy when the technology did become available it would be too late in the development schedule to spend time running test chips the yield analysis had to be done analytically or by simulation analytic yield analysis techniques did not offer sufficient accuracy for dealing with complex structures the simulation techniques then available were very labor intensive and seemed more suitable for redundant memories and other very regular structures stapper 80j i wanted a simulator that would allow me to evaluate the yield of arbitrary redundant layouts hence i termed such a simulator a layout or yield simulator since i was unable to convince anyone to build such a simulator for me i embarked on the research myself

vlsi systems are becoming very complex and difficult to test traditional stuck at fault problems may be inadequate to model possible manufacturing defects in the integrated ciruit hierarchial models are needed that are easy to use at the transistor and functional levels stuck open faults present severe testing problems in cmos circuits to overcome testing problems testable designs are utilized bridging faults are important due to the shrinking geometry of ics bist pla schemes have common features controllability and observability which are enhanced through additional logic and test points certain circuit topologies are more easily testable than others the amount of reconvergent fan out is a critical factor in determining realistic measures for determining test generation difficulty test implementation is usually left until after the vlsi data path has been synthesized into a structural description this leads to investigation methodologies for performing design synthesis with test incorporation these topics and more are discussed

the vhsic hardware description language vhdl provides a standard machine processable notation for describing hardware vhdl is the result of a collaborative effort between ibm intermetrics and texas instruments sponsored by the very high speed integrated cir cuits vhsic program office of the department of defense beginning in 1981 today it is an ieee standard 1076 1987 and several simulators and other automated support tools for it are available commercially by providing a standard notation for describing hardware especially in the early stages of the hardware design process vhdl is expected to reduce both the time lag and the cost involved in building new systems and upgrading existing ones vhdl is the result of an evolutionary approach to language devel opment starting with high level hardware description languages existing in 1981 it has a decidedly programming language flavor resulting both from the orientation of hardware languages of that time and from a ma jor requirement that vhdl use ada constructs wherever appropriate during the 1980 s there has been an increasing current of research into high level specification languages for systems particularly in the software area and new methods of utilizing specifications in systems de velopment this activity is worldwide and includes for example object oriented design various rigorous development methods mathematical verification and synthesis from high level specifications val vhdl annotation language is a simple further step in the evolution of hardware description languages in the direction of applying new methods that have developed since vhdl was designed

as mos devices are scaled to meet increasingly demanding circuit specifications process variations have a greater effect on the reliability of circuit performance for this reason statistical techniques are required to design integrated circuits with maximum yield statistical modeling for computer aided design of mos vlsi circuits describes a statistical circuit simulation and optimization environment for vlsi circuit designers the first step toward accomplishing statistical circuit design and optimization is the development of an accurate cad tool capable of performing statistical simulation this tool must be based on a statistical model which comprehends the effect of device and circuit characteristics such as device size bias and circuit layout which are under the control of the circuit designer on the variability of circuit performance the distinctive feature of the cad tool described in this book is its ability to accurately model and simulate the effect in both intra and inter die process variability on analog digital circuits accounting for the effects of the aforementioned device and circuit characteristics statistical modeling for computer aided design of mos vlsi circuits serves as an excellent reference for those working in the field and may be used as the text for an advanced course on the subject

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