

Chip Design For Submicron Vlsi Cmos Layout And

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Chip Design For Submicron Vlsi: Cmos Layout & Simulation
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VLSI Design
Low Power High Performance VLSI Design in Deep-submicron CMOS Processes
Proceedings of the Ninth Asian Test Symposium
Device Design and Process
Window Analysis of a Deep Submicron CMOS VLSI Technology
Electron-beam, X-ray, & Ion-beam Techniques for Submicrometer Lithographies
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Design of High-Performance Microprocessor Circuits
John Paul Uyemura Umura Xueping Jiang Faith Hamzaoglu Philip E. Madrid Phillip D. Blais James B. Kuo
IEEE Circuits and Systems Society Institute of Electrical and Electronics Engineers
Centre national d'études spatiales (France)
Electrochemical Society Anantha Chandrakasan
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this book teaches the principles of physical design layout and simulation of cmos integrated circuits it is written around a very powerful cad program called microwind that is available on the accompanying cd rom featuring a friendly interface microwind is both educational and useful for designing cmos chips

these conference proceedings cover such topics as analogue and mixed signal tests memory built in self test and self diagnosis fault simulation and timing simulation fault analysis test generation functional testing and memory testing

these volumes relate to matters discussed during the 2003 ieee international symposium on circuits and systems such as analogue circuits and signal processing communications multimedia systems and applications general and nonlinear circuits and systems and neural networks and systems

the authors present readers with a compelling one stop advanced system perspective on the intrinsic issues of digital system design this invaluable reference prepares

readers to meet the emerging challenges of the device and circuit issues associated with deep submicron technology it incorporates future trends with practical contemporary methodologies

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