

## Auditing A Business Risk Approach 8th

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the results are summarized of a program to demonstrate the feasibility of bubble domain memory technology as a mass memory medium for spacecraft applications the design fabrication and test of a partially populated 10 to the 8th power bit data recorder using 100 kbit serial bubble memory chips is described design tradeoffs design approach and performance are discussed this effort resulted in a 10 to the 8th power bit recorder with a volume of 858 6 cu in and a weight of 47 2 pounds the recorder is plug reconfigurable having the capability of operating as one two or four independent serial channel recorders or as a single sixteen bit byte parallel input recorder data rates up to 1 2 mb s in a serial mode and 2 4 mb s in a parallel mode may be supported fabrication and test of the recorder demonstrated the basic feasibility of bubble domain memory technology for such applications test results indicate the need for improvement in memory element operating temperature range and detector performance

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