

Finite State Machines In Hardware Theory And Design With Vhdl And Systemverilog

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a comprehensive guide to the theory and design of hardware implemented finite state machines with design examples developed in both vhdl and systemverilog languages modern complex digital systems invariably include hardware implemented finite state machines the correct design of such parts is crucial for attaining proper system performance this book offers detailed comprehensive coverage of the theory and design for any category of hardware implemented finite state machines it describes crucial design problems that lead to incorrect or far from optimal implementation and provides examples of finite state machines developed in both vhdl and systemverilog the successor of verilog hardware description languages important features include extensive review of design practices for sequential digital circuits a new division of all state machines into three hardware based categories encompassing all possible situations with numerous practical examples provided in all three categories the presentation of complete designs with detailed vhdl and systemverilog codes

comments and simulation results all tested in fpga devices and exercise examples all of which can be synthesized simulated and physically implemented in fpga boards additional material is available on the book s website designing a state machine in hardware is more complex than designing it in software although interest in hardware for finite state machines has grown dramatically in recent years there is no comprehensive treatment of the subject this book offers the most detailed coverage of finite state machines available it will be essential for industrial designers of digital systems and for students of electrical engineering and computer science

synthesis of finite state machines functional optimization is one of two monographs devoted to the synthesis of finite state machines fsms this volume addresses functional optimization whereas the second addresses logic optimization by functional optimization here we mean the body of techniques that compute all permissible sequential functions for a given topology of interconnected fsms and select a best sequential function out of the permissible ones the result is a symbolic description of the fsm representing the chosen sequential function by logic optimization here we mean the steps that convert a symbolic description of an fsm into a hardware implementation with the goal to optimize objectives like area testability performance and so on synthesis of finite state machines functional optimization is divided into three parts the first part presents some preliminary definitions theories and techniques related to the exploration of behaviors of fsms the second part presents an implicit algorithm for exact state minimization of incompletely specified finite state machines isfsms and an exhaustive presentation of explicit and implicit algorithms for the binate covering problem the third part addresses the computation of permissible behaviors at a node of a network of fsms and the related minimization problems of non deterministic finite state machines ndfsms key themes running through the book are the exploration of behaviors contained in a non deterministic fsm ndfsm and the representation of combinatorial problems arising in fsm synthesis by means of binary decision diagrams bdds synthesis of finite state machines functional optimization will be of interest to researchers and designers in logic synthesis cad and design automation

presents the fundamentals design of microcoded systems starting from simple state machines using a progression of four built tested circuits a basic rom based state machine a state machine with an alu registers a simple cpu with an 8 bit data bus a 16 bit address bus a bit slice based cpu that allows interrupts bus sharing asynchronous data transfers all circuits are built using real devices with reference made to real data manuals giving the text a more practical slant

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